of memory system 100.

Please add the following paragraph to the specification at page 5, line 21:

Figure 6 is a block diagram of a dynamic random access memory device.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 29, 32, 38, 40, 42, 44, 48, 52, 63, and 67. The specific amendments to individual claims are detailed in the following marked up set of claims.

29. (Amended) A method of retrieving data in a pipelined memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing commands and addresses on a unidirectional command and address bus;

latching the commands and addresses in the command buffers;

driving the latched commands and addresses to the column and row decoders;

retrieving data from the addressable storage of one of the plurality of memory devices;

latching the data in the data in and data out buffer of the one of the plurality of memory devices;

latching the data in the data buffer of the one memory [device] subsystem; and

receiving the data on a bidirectional data bus.

32. (Amended) A method of storing data in a pipelined memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing commands and addresses on a unidirectional command and address bus;

issuing data on a bidirectional data bus;

latching the commands and addresses in the plurality of command buffers;

latching the data in the plurality of data buffers of the memory subsystem;

driving the latched commands and addresses to the column and row decoders;

driving the latched data to the data in buffers of the memory device; and

storing the data in the addressable storage of the plurality of memory devices.

38. (Amended) A method of performing a memory transaction in an electronic system having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device includes a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing information to the memory controller;

issuing commands and addresses on a unidirectional command and address bus;

issuing data on a bidirectional data bus;

latching the commands and addresses received from the unidirectional command and address bus in the command buffers of the plurality of memory subsystems;

driving the latched commands and addresses to the plurality of memory devices; and

if the memory transaction is a write, receiving and latching the data in the data buffers of the plurality of memory subsystems, [and] driving the latched data to the data in and data out buffer, and writing the data to an addressed memory storage of the plurality of memory devices.

40. (Amended) A method of storing data, in an electronic system, having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device includes a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses on a unidirectional command and address bus;

issuing data on a bidirectional data bus;

latching the commands and addresses read from the unidirectional command and address bus in the command buffers of the plurality of memory subsystems;

latching the data received from the bidirectional data bus in the data buffers of the plurality of memory subsystems;

driving the latched commands and addresses to the plurality of memory devices;

driving the latched data to the data in and data out buffer of the plurality of memory devices; and

storing the data from the data in and data out buffer in addressable storage of the plurality of memory devices.

42. (Amended) In an electronic system having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device includes a data in and a data out buffer, a column decoder and a row decoder, a method of retrieving data comprising:

issuing information to the memory controller;

issuing commands and addresses on a unidirectional command and address bus;

latching the commands and addresses read from the unidirectional command and address bus in the command buffers of the plurality of memory subsystems;

driving the latched commands and addresses to the plurality of memory devices of the plurality of memory subsystems;

retrieving data from addressable storage of the plurality of memory devices of the plurality of memory subsystems;

latching the data in the data in and data out buffer of a memory storage device;

latching the data in the data buffers of the plurality of memory devices of the plurality of memory subsystems; and

receiving the data on a bidirectional data bus.

44. (Amended) A memory system comprising:

a unidirectional command and address bus coupleable to a memory control device;

a bidirectional data bus coupleable to the memory control device; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

a command buffer connected between the command and address bus and the plurality of memory devices, the command buffer receiving and latching commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices, wherein the command buffer is shared by the plurality of memory devices; and

a data buffer connected between the plurality of memory devices and the bidirectional data bus, the data buffer receiving and latching data information from the bidirectional data bus and driving the data information to data in and data out buffer of the plurality of memory devices for a write operation, the data buffer receiving and latching the data information from the data in and data out buffer of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

48. (Amended) A method of storing data in a pipeline memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

receiving commands and addresses from a unidirectional command and address bus;

receiving data from a bidirectional data bus;

latching the commands and addresses in the plurality of command buffers;

latching the data in the plurality of data buffers;

driving the latched commands and addresses to the column and row decoders;

driving the latched data to the data in buffers; and

storing the data latched in the data in buffer in the addressable storage of the plurality of memory devices.

50. (Amended) A method of retrieving data in a pipeline memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

receiving commands and addresses from a unidirectional command and address bus;

latching the commands and addresses in the plurality of command buffers;

driving the latched commands and addresses to the column and row decoders;

retrieving data from the addressable storage of the plurality of memory devices;

latching the data in the data in and data out buffer of the memory device;

latching the data from the data in and data out buffer in the plurality of data buffers; and

driving the data from the data in and data out buffer onto a data bus.

52. (Amended) A memory system, comprising:

a unidirectional command and address bus in electrical communication with a memory control device;

a bidirectional data bus in electrical communication with the memory control device; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

a command buffer connected between the command and address bus and the plurality of memory devices, the command buffer receiving and latching commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices, wherein the command buffer is shared by the plurality of memory devices; and

a data buffer connected between the data in and data out buffer of each of the plurality of memory devices and the bidirectional data bus, the data buffer receiving and

latching data information from the bidirectional data bus and driving the data information to the data in and data out buffer of the plurality of memory devices for a write operation, the data buffer receiving and latching the data information from the data in and data out buffer of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

63. (Amended) A method of operating the memory system of claim 5, comprising:
issuing commands and addresses on the unidirectional command and address bus;
latching the commands and addresses in the command buffers;
driving the latched commands and addresses to the column and row decoders;
retrieving data from addressable storage of one of the plurality of memory devices;
latching the data in the data in and dat out buffers;
latching the data from the data in and data out buffer in the data buffers; and
receiving the data on the bidirectional data bus.

67. (Amended) A memory system comprising:
a memory controller;
a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;
a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation; and
a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:
a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;
a command buffer connected between the command and address bus and the plurality of memory devices, the command buffer receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and